EAST SEARCH

8/4/05

L#	Hits	Search String	Databases
S1	3374	((Integrated or digital) near2 circuit$1) and netlist	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S2	99	S1 and (edit$3 with netlist$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S3	348	S1 and (netlist$1 with module$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S4	587	S1 and (netlist$1 with (chang$3 or modif$4 or modification))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S5	3	S1 and (netlist$1 with modifier$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S6	820	S1 and (netlist$1 with ("hardware description language" or HDL or VHDL or verilog))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S7	579	S1 and (netlist$1 with ("hardware description language" or VHDL or verilog))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S8	193	S1 and (netlist$1 with object$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S9	758	S1 and (netlist$1 with element$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S10	558	S1 and (netlist$1 with representation$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S11	1	S1 and (netlist$1 with representational)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S12	10	S1 and (netlist$1 with compliler)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S13	185	S1 and (module with port$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S14	141	S1 and (configuration with port$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S15	114	S1 and (wire with port$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S16	445	S1 and (netlist$1 with (hierarchical or hierarchy))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S17	167	S1 and (netlist$1 with (hierarchical or hierarchy) with level$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S18	146	S1 and (instance with port$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S19	2	S1 and (instance with modifier$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S20	2	S1 and (element$1 with modifier$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S21	1	S1 and (attribute$1 with modifier$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S22	1	S1 and (port$1 with modifier$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S23	201	S1 and (port$1 with netlist$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S24	3	S1 and (object-based with netlist$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S25	100	S3 and S4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S26	80	S3 and S7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S27	57	S3 and S8	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S28	127	S3 and S9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S29	132	S3 and S10	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S30	23	S13 and S14	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S31	111	S3 and S13	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S32	11	S3 and S14	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S33	24	S13 and S15	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S34	50	S3 and S17	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S35	32	S13 and S18	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S36	31	S3 and S18	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S37	45	S13 and S23	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S38	388	S2 or S5 or S12 or S19 or S20 or S21 or S22 or S24 or S25 or S26 or S27 or S28 or S29 or S30	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S39	272	S2 or S5 or S12 or S19 or S20 or S21 or S22 or S24 or S26 or S27 or S30 or S32 or S33 or S34	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

S40	349	S15 or S25 or S28 or S29 or S31	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S41	157	S39 and S40	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S42	272	S39 or S41	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S43	3380	((Integrated or digital) near2 circuit$1) and netlist	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S44	1	S43 and (definitional with modifier$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S46	348	S43 and (netlist$1 with module$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S48	582	S43 and (netlist$1 with ("hardware description language" or VHDL or verilog))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S49	194	S43 and (netlist$1 with object$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S51	185	S43 and (module with port$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S52	141	S43 and (configuration with port$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S53	114	S43 and (wire with port$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S54	168	S43 and (netlist$1 with (hierarchical or hierarchy) with level$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S55	146	S43 and (instance with port$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S56	2	S43 and (instance with modifier$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S57	2	S43 and (element$1 with modifier$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S58	1	S43 and (attribute$1 with modifier$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S59	1	S43 and (port$1 with modifier$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S60	202	S43 and (port$1 with netlist$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S61	3	S43 and (object-based with netlist$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S62	80	S46 and S48	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S63	57	S46 and S49	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S64	23	S51 and S52	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S67	50	S46 and S54	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S69	31	S46 and S55	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S70	45	S51 and S60	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S71	272	S45 or S47 or S50 or S56 or S57 or S58 or S59 or S61 or S62 or S63 or S64 or S65 or S66 or S	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S72	588	S43 and (netlist$1 with (chang$3 or modif$4 or modification))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S73	761	**S43 and (netlist$1 with element$1)**	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S74	559	S43 and (netlist$1 with representation$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S75	100	S46 and S72	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S76	127	S46 and S73	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S77	132	S46 and S74	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S78	111	S46 and S51	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S79	349	S53 or S75 or S76 or S77 or S78	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S80	157	S71 and S79	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S81	272	S71 or S80	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S45	99	S43 and (edit$3 with netlist$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S47	3	S43 and (netlist$1 with modifier$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S50	10	S43 and (netlist$1 with compliler)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S65	11	S46 and S52	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S66	24	S51 and S53	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S68	32	S51 and S55	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S82	3382	((Integrated or digital) near2 circuit$1) and netlist	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S83	1	S82 and (definitional with modifier$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S84	99	S82 and (edit$3 with netlist$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S85	348	S82 and (netlist$1 with module$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

S86	3	S82 and (netlist$1 with modifier$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S87	582	S82 and (netlist$1 with ("hardware description language" or VHDL or verilog))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S88	194	S82 and (netlist$1 with object$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S89	10	S82 and (netlist$1 with compliler)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S90	185	S82 and (module with port$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S91	141	S82 and (configuration with port$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S92	114	S82 and (wire with port$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S93	168	S82 and (netlist$1 with (hierarchical or hierarchy) with level$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S94	146	S82 and (instance with port$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S95	2	S82 and (instance with modifier$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S96	2	S82 and (element$1 with modifier$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S97	1	S82 and (attribute$1 with modifier$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S98	1	S82 and (port$1 with modifier$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S99	202	S82 and (port$1 with netlist$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S100	3	S82 and (object-based with netlist$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S101	80	S85 and S87	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S102	57	S85 and S88	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S103	23	S90 and S91	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S104	11	S85 and S91	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S105	24	S90 and S92	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S106	50	S85 and S93	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S107	32	S90 and S94	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S108	31	S85 and S94	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S109	45	S90 and S99	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S110	272	S84 or S86 or S89 or S95 or S96 or S97 or S98 or S100 or S101 or S102 or S103 or S104 or S1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S111	588	S82 and (netlist$1 with (chang$3 or modif$4 or modification))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S112	761	S82 and (netlist$1 with element$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S113	559	S82 and (netlist$1 with representation$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S114	100	S85 and S111	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S115	127	S85 and S112	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S116	132	S85 and S113	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S117	111	S85 and S90	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S118	349	S92 or S114 or S115 or S116 or S117	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S119	157	S110 and S118	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S120	272	S110 or S119	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S121	299	S82 and (wire with (chang$3 or modif$4 or modification))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S122	124	S82 and (port with (chang$3 or modif$4 or modification))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S123	8	S121 and S122	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S124	3	S82 and (wire with port with (chang$3 or modif$4 or modification))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S125	79	S82 and (attribute$1 with (chang$3 or modif$4 or modification))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S126	11	S82 and (attribute$1 with (netlist or element) with(chang$3 or modif$4 or modification))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

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Results of search set S115

Document IKind Codes	Title	Issue Date	Current OR	Abstract
US 20050137841 A1	Embedding keys into test data	20050623	703/14	
US 20050131666 A1	Circuit simulation bus transaction analysis	20050616	703/17	
US 20050125758 A1	Positioning of inverting buffers in a netlist	20050609	716/10	
US 20050108672 A1	Method of generating a physical netlist for a hierarchical integrated circuit design	20050519	716/12	
US 20050097493 A1	Gate reuse methodology for diffused cell-based IP blocks in platform-based silicon products	20050505	716/11	
US 20050091627 A1	Comparison of two hierarchical netlist to generate change orders for updating an integrated circuit	20050428	716/12	
US 20050080953 A1	Fragment storage for data alignment and merger	20050414	710/52	
US 20050080952 A1	Descriptor-based load balancing	20050414	710/52	
US 20050078696 A1	Descriptor write back delay mechanism to improve performance	20050414	370/419	
US 20050078694 A1	Packet manager interrupt mapper	20050414	370/412	
US 20050078669 A1	Exponential channelized timer	20050414	370/389	
US 20050078601 A1	Hash and route hardware with parallel routing scheme	20050414	370/218	
US 20050050506 A1	System and method for determining connectivity of nets in a hierarchical circuit design	20050303	716/12	
US 20050050488 A1	System and method for determining a highest level signal name in a hierarchical VLSI design	20050303	716/4	
US 20050038928 A1	Distributed configuration storage	20050217	710/8	
US 20050033870 A1	Distributed configuration storage	20050210	710/8	
US 20050027491 A1	Symbolic analysis of electrical circuits for application in telecommunications	20050203	702/196	
US 20040230920 A1	Method and apparatus for implementing engineering change orders	20041118	716/1	
US 20040225490 A1	Device for emulating one or more integrated-circuit chips	20041111	703/27	
US 20040207429 A1	Semiconductor integrated circuit and circuit design apparatus	20041021	326/40	
US 20040194048 A1	System and method for efficiently mapping heterogeneous objects onto an array of heterogeneous	20040930	716/17	
US 20040186703 A1	System and method for estimating power consumption for at least a portion of an integrated circui	20040923	703/18	
US 20040163067 A1	Method and apparatus for layout of high speed digital logic for datapath portions of microprocessc	20040819	716/10	
US 20040158789 A1	Using pseudo-pins in generating scan test vectors for testing an embedded core while maintainin	20040812	714/741	
US 20040128641 A1	Simplified process to design integrated circuits	20040701	716/18	
US 20040128626 A1	Placement of configurable input/output buffer structures during design of integrated circuits	20040701	716/1	
US 20040123258 A1	Logic multiprocessor for FPGA implementation	20040624	716/5	
US 20040122990 A1	Distributed configuration storage	20040624	710/8	
US 20040117756 A1	Methods and apparatuses for designing integrated circuits	20040617	716/18	
US 20040115995 A1	Circuit array module	20040617	439/701	
US 20040111252 A1	Method and system for emulating a design under test associated with a test environment	20040610	703/28	
US 20040073876 A1	Method and apparatus for enhancing the performance of event driven dynamic simulation of digita	20040415	716/6	
US 20040025136 A1	Method for designing a custom ASIC library	20040205	716/17	
US 20040021490 A1	Method and apparatus for timing management in a converted design	20040205	327/165	
US 20040002846 A1	Transistor level verilog	20040101	703/19	
US 20030229872 A1	Simulation result verification method and simulation result verification device	20031211	716/6	
US 20030229870 A1	Systems and methods for performing clock gating checks	20031211	716/6	
US 20030208721 A1	Apparatus and method to facilitate hierarchical netlist checking	20031106	716/1	
US 20030204822 A1	Digital logic optimization using selection operators	20031030	716/2	
US 20030200510 A1	Digital circuits using universal logic gates	20031023	716/1	
US 20030200070 A1	Simulation of uncharacterized hardware	20031023	703/14	

US 20030188268 A1	Low Vt transistor substitution in a semiconductor device	20031002	716/2
US 20030177457 A1	Optimization of digital designs	20030918	716/3
US 20030177427 A1	Circuit modeling	20030918	714/741
US 20030149954 A1	Methods and apparatuses for designing integrated circuits	20030807	716/18
US 20030149953 A1	Integrated circuit cell library	20030807	716/17
US 20030149859 A1	Digital circuit implementation by means of parallel sequencers	20030807	712/21
US 20030145288 A1	Method and apparatus for improving digital circuit design	20030731	716/2
US 20030139842 A1	Fast algorithm to extract flat information from hierarchical netlists	20030724	700/182
US 20030126579 A1	Digital design using selection operations	20030703	716/18
US 20030125925 A1	Batch editor for netlists described in a hardware description language	20030703	703/22
US 20030121013 A1	Timing model extraction by timing graph reduction	20030626	716/6
US 20030120474 A1	Assertion handling for timing model extraction	20030626	703/19
US 20030101331 A1	ASIC design technique	20030529	712/36
US 20030084416 A1	Scalable, partitioning integrated circuit layout system	20030501	716/7
US 20030084410 A1	SPICE to Verilog netlist translator	20030501	716/3
US 20030079195 A1	Methods and apparatuses for designing integrated circuits	20030424	716/8
US 20030079192 A1	METHOD FOR GENERATING A PARTITIONED IC LAYOUT	20030424	716/7
US 20030033595 A1	Automated HDL modifying apparatus and computer-readable recording medium in which prograr	20030213	717/143
US 20030014703 A1	Using pseudo-pins in generating scan test vectors for testing an embedded core while maintainin	20030116	714/726
US 20030009734 A1	Method for generating design constraints for modules in a hierarchical integrated circuit design sy	20030109	716/6
US 20030009727 A1	Circuit designing apparatus, circuit designing method and timing distribution apparatus	20030109	716/1
US 20020194575 A1	Hierarchical layout method for integrated circuits	20021219	716/17
US 20020194572 A1	Methods and apparatuses for designing integrated circuits	20021219	716/1
US 20020183997 A1	Apparatus and method for specifying the configuration of mixed-language simulation models	20021205	703/13
US 20020170037 A1	Apparatus and method for controlling event ordering in a mixed- language simulator	20021114	717/131
US 20020166110 A1	Apparatus and method for performing event processing in a mixed-language simulator	20021107	717/106
US 20020156609 A1	Circuit simulation method, circuit simulation device, and circuit simulation program and computer	20021024	703/14
US 20020147576 A1	System for characterizing simulated circuit logic and behavior	20021010	703/15
US 20020145433 A1	An algorithm for finding vectors to stimulate all paths and arcs through an LVS gate	20021010	324/530
US 20020138817 A1	Method for inserting antenna diodes into an integrated circuit design	20020926	716/12
US 20020129334 A1	Interface based design using a tabular paradigm	20020912	717/123
US 20020083398 A1	Circuit designing apparatus, circuit designing method and timing distribution apparatus	20020627	716/1
US 20020073380 A1	Block based design methodology with programmable components	20020613	716/1
US 20020045995 A1	Electromagnetic interference analysis method and apparatus	20020418	702/77
US 20020038401 A1	Design tool for systems-on-a-chip	20020328	710/305
US 20020023107 A1	Schematic organization tool	20020221	715/504
US 20020018583 A1	Advanced schematic editor	20020214	382/113
US 20010047509 A1	Modular design method and system for programmable logic devices	20011129	716/18
US 20010034873 A1	Device level layout optimization in electronic design automation	20011025	716/8
US 20010001881 A1	Methods and media for utilizing symbolic expressions in circuit modules	20010524	716/1
US 6915410 B2	Compiler synchronized multi-processor programmable logic device with direct transfer of computa	20050705	712/17
US 6904571 B1	Algorithm and methodology for the polygonalization of sparse circuit schematics	20050607	716/2
US 6892373 B2	Integrated circuit cell library	20050510	716/17
US 6886140 B2	Fast algorithm to extract flat information from hierarchical netlists	20050426	716/1
US 6877150 B1	Method of transforming software language constructs to functional hardware equivalents	20050405	716/18
US 6876961 B1	Electronic system modeling using actual and approximated system properties	20050405	703/19

US 6872601 B1	Method and apparatus for timing management in a converted design	20050329	438/129
US 6868534 B2	Circuit modeling	20050315	716/6
US 6868531 B1	Generation of ordered interconnect output from an HDL representation of a circuit	20050315	716/1
US 6865726 B1	IC layout system employing a hierarchical database by updating cell library	20050308	716/18
US 6857110 B1	Design methodology for merging programmable logic into a custom IC	20050215	716/4
US 6856950 B1	Abstract verification environment	20050215	703/13
US 6848084 B1	Method and apparatus for verification of memories at multiple abstraction levels	20050125	716/1
US 6845494 B2	Method for generating design constraints for modules in a hierarchical integrated circuit design sy	20050118	716/6
US 6836877 B1	Automatic synthesis script generation for synopsys design compiler	20041228	716/18
US 6823502 B2	Placement of configurable input/output buffer structures during design of integrated circuits	20041123	716/9
US 6817005 B2	Modular design method and system for programmable logic devices	20041109	716/16
US 6792589 B2	Digital design using selection operations	20040914	716/18
US 6792579 B2	Spice to verilog netlist translator and design methods using spice to verilog and verilog to spice tra	20040914	716/3
US 6779158 B2	Digital logic optimization using selection operators	20040817	716/3
US 6779156 B2	Digital circuits using universal logic gates	20040817	716/1
US 6769107 B1	Method and system for implementing incremental change to circuit design	20040727	716/16
US 6745371 B2	Low Vt transistor substitution in a semiconductor device	20040601	716/2
US 6745358 B1	Enhanced fault coverage	20040601	714/726
US 6738957 B2	Schematic organization tool	20040518	716/11
US 6721926 B2	Method and apparatus for improving digital circuit design	20040413	716/2
US 6697982 B2	Generating netlist test vectors by stripping references to a pseudo input	20040224	714/738
US 6684373 B1	Optimize global net timing with repeater buffers	20040127	716/6
US 6678871 B2	Circuit designing apparatus, circuit designing method and timing distribution apparatus	20040113	716/6
US 6675366 B1	System and method for disabling schematics	20040106	716/11
US 6671868 B1	Method of creating MCM pinouts	20031230	716/16
US 6671866 B2	Device level layout optimization in electronic design automation	20031230	716/10
US 6668364 B2	Methods and apparatuses for designing integrated circuits	20031223	716/7
US 6668362 B1	Hierarchical verification for equivalence checking of designs	20031223	716/5
US 6658630 B1	Method to translate UDPs using gate primitives	20031202	716/3
US 6658628 B1	Developement of hardmac technology files (CLF, tech and synlib) for RTL and full gate level netlis	20031202	716/1
US 6651235 B2	Scalable, partitioning integrated circuit layout system	20031118	716/7
US 6651232 B1	Method and system for progressive clock tree or mesh construction concurrently with physical des	20031118	716/7
US 6634008 B1	Methodology server based integrated circuit design	20031014	716/1
US 6625787 B1	Method and apparatus for timing management in a converted design	20030923	716/6
US 6618834 B2	Circuit designing apparatus, circuit designing method and timing distribution apparatus	20030909	716/2
US 6601024 B1	Code translation between hardware design languages	20030729	703/14
US 6591402 B1	System and method for performing assertion-based analysis of circuit designs	20030708	716/5
US 6578183 B2	Method for generating a partitioned IC layout	20030610	716/7
US 6578133 B1	MIMD array of single bit processors for processing logic equations in strict sequential order	20030610	712/21
US 6574787 B1	Method and apparatus for logic synthesis (word oriented netlist)	20030603	716/18
US 6574779 B2	Hierarchical layout method for integrated circuits	20030603	716/1
US 6557156 B1	Method of configuring FPGAS for dynamically reconfigurable computing	20030429	716/17
US 6557149 B2	Algorithm for finding vectors to stimulate all paths and arcs through an LVS gate	20030429	716/4
US 6546536 B1	System and method for disabling schematics	20030408	716/11
US 6539536 B1	Electronic design automation system and methods utilizing groups of multiple cells having loop-ba	20030325	716/18
US 6539520 B1	Systems and methods for generating hardware description code	20030325	716/3

US 6536028 B1	Standard block architecture for integrated circuit design	20030318	716/17
US 6536018 B1	Reverse engineering of integrated circuits	20030318	716/4
US 6530065 B1	Client-server simulator, such as an electrical circuit simulator provided by a web server over the in	20030304	716/4
US 6526554 B1	Integrated circuit layout system, integrated circuit layout method, and computer-readable storage r	20030225	716/10
US 6519755 B1	Method and apparatus for logic synthesis with elaboration	20030211	716/18
US 6519754 B1	Methods and apparatuses for designing integrated circuits	20030211	716/18
US 6519749 B1	Integrated circuit partitioning placement and routing system	20030211	716/9
US 6510548 B1	Method for providing pre-designed modules for programmable logic devices	20030121	716/16
US 6510546 B1	Method and apparatus for pre-routing dynamic run-time reconfigurable logic cores	20030121	716/16
US 6510542 B1	Method of placing a repeater cell in an electricalcircuit	20030121	716/10
US 6502229 B2	Method for inserting antenna diodes into an integrated circuit design	20021231	716/12
US 6499125 B1	Method for inserting test circuit and method for converting test data	20021224	714/734
US 6496955 B1	Latch mapper	20021217	716/3
US 6493864 B1	Integrated circuit block model representation hierarchical handling of timing exceptions	20021210	716/18
US 6493648 B1	Method and apparatus for logic synthesis (inferring complex components)	20021210	702/119
US 6490717 B1	Generation of sub-netlists for use in incremental compilation	20021203	716/18
US 6480995 B1	Algorithm and methodology for the polygonalization of sparse circuit schematics	20021112	716/11
US 6467074 B1	Integrated circuit architecture with standard blocks	20021015	716/17
US 6463568 B1	Apparatus and method for designing a circuit using minimum slice construction and replication	20021008	716/2
US 6457164 B1	Hetergeneous method for determining module placement in FPGAs	20020924	716/8
US 6446251 B1	Method and apparatus for socket-based design with reusable-IP	20020903	716/18
US 6438735 B1	Methods and apparatuses for designing integrated circuits	20020820	716/7
US 6421818 B1	Efficient top-down characterization method	20020716	716/18
US 6405356 B1	Method of automatic placement for an arrayed-element device	20020611	716/10
US 6401231 B1	Method and apparatus for performing both negative and positive slack time budgeting and for dete	20020604	716/6
US 6378123 B1	Method of handling macro components in circuit design synthesis	20020423	716/18
US 6374205 B1	Method of reducing circuit data, method of simulating circuit, and medium for storing circuit data r	20020416	703/14
US 6366874 B1	System and method for browsing graphically an electronic design based on a hardware descriptio	20020402	703/14
US 6360353 B1	Automated alternating current characterization testing	20020319	716/4
US 6360191 B1	Method and apparatus for automated design of complex structures using genetic programming	20020319	703/6
US 6353915 B1	Methods for evaluating systems of electronic components	20020305	716/4
US 6345378 B1	Synthesis shell generation and use in ASIC design	20020205	716/2
US 6339836 B1	Automated design partitioning	20020115	716/5
US 6327556 B1	AT-speed computer model testing methods	20011204	703/13
US 6304837 B1	Automated test vector generation and verification	20011016	703/14
US 6298319 B1	Incremental compilation of electronic design for work group	20011002	703/26
US 6295636 B1	RTL analysis for improved logic synthesis	20010925	716/18
US 6292931 B1	RTL analysis tool	20010918	716/18
US 6292925 B1	Context-sensitive self implementing modules	20010918	716/8
US 6289498 B1	VDHL/Verilog expertise and gate synthesis automation system	20010911	716/18
US 6289491 B1	Netlist analysis tool by degree of conformity	20010911	716/5
US 6272665 B1	Method and tool for automatically generating engineering change order	20010807	716/3
US 6263483 B1	Method of accessing the generic netlist created by synopsys design compilier	20010717	716/18
US 6260182 B1	Method for specifying routing in a logic module by direct module communication	20010710	716/12
US 6249902 B1	Design hierarchy-based placement	20010619	716/10
US 6243851 B1	Heterogeneous method for determining module placement in FPGAs	20010605	716/10

US 6243849 B1	Method and apparatus for netlist filtering and cell placement	20010605	716/8
US 6230304 B1	Method of designing a constraint-driven integrated circuit layout	20010508	716/7
US 6216259 B1	Configuration of programmable logic devices with routing core generators	20010410	716/17
US 6216258 B1	FPGA modules parameterized by expressions	20010410	716/17
US 6212655 B1	IDDQ test solution for large asics	20010403	714/724
US 6205572 B1	Buffering tree analysis in mapped design	20010320	716/5
US 6202044 B1	Concurrent hardware-software co-simulation	20010313	703/28
US 6182269 B1	Method and device for fast and accurate parasitic extraction	20010130	716/5
US 6175946 B1	Method for automatically generating checkers for finding functional defects in a description of a ci	20010116	716/4
US 6173435 B1	Internal clock handling in synthesis script	20010109	716/18
US 6167555 A	System and method for converting polygon-based wires of an integrated circuit design to path-bas	20001226	716/3
US 6134705 A	Generation of sub-netlists for use in incremental compilation	20001017	716/18
US 6120549 A	Method and apparatus for generating optimized functional macros	20000919	703/20
US 6108494 A	Optimizing runtime communication processing between simulators	20000822	703/14
US 6106568 A	Hierarchical scan architecture for design for test applications	20000822	716/18
US 6102964 A	Fitting for incremental compilation of electronic designs	20000815	716/18
US 6080204 A	Method and apparatus for contemporaneously compiling an electronic circuit design by contempo	20000627	716/7
US 6078736 A	Method of designing FPGAs for dynamically reconfigurable computing	20000620	716/16
US 6067650 A	Method and apparatus for performing partial unscan and near full scan within design for test appli	20000523	714/726
US 6064806 A	System and method for converting a polygon-based layout of an integrated circuit design to an obj	20000516	716/3
US 6058252 A	System and method for generating effective layout constraints for a circuit design or the like	20000502	716/10
US 6014506 A	Method and apparatus for improving engineering change order placement in integrated circuit des	20000111	716/11
US 6002861 A	Method for performing simulation using a hardware emulation system	19991214	703/16
US 5991523 A	Method and system for HDL global signal simulation and verification	19991123	716/18
US 5983277 A	Work group computing for electronic design automation	19991109	709/232
US 5963454 A	Method and apparatus for efficiently implementing complex function blocks in integrated circuit de	19991005	716/18
US 5949692 A	Hierarchical scan architecture for design for test applications	19990907	716/18
US 5946478 A	Method for generating a secure macro element of a design for a programmable IC	19990831	716/17
US 5940603 A	Method and apparatus for emulating multi-ported memory circuits	19990817	716/5
US 5937179 A	Integrated circuit design system with shared hardware accelerator and processes of designing int	19990810	716/16
US 5920830 A	Methods and apparatus for generating test vectors and validating ASIC designs	19990706	702/119
US 5903466 A	Constraint driven insertion of scan logic for implementing design for test within an integrated circu	19990511	716/18
US 5894420 A	Method for spawning two independent states in a state flow diagram	19990413	716/12
US 5875112 A	Methods for implementing circuit designs in physical circuits	19990223	716/12
US 5867397 A	Method and apparatus for automated design of complex structures using genetic programming	19990202	703/14
US 5857109 A	Programmable logic device for real time video processing	19990105	712/37
US 5850537 A	Pipe lined static router and scheduler for configurable logic system performing simultaneous comi	19981215	716/12
US 5841663 A	Apparatus and method for synthesizing integrated circuits using parameterized HDL modules	19981124	716/18
US 5831869 A	Method of compacting data representations of hierarchical logic designs used for static timing ana	19981103	716/6
US 5831868 A	Test ready compiler for design for test synthesis	19981103	716/18
US 5828588 A	Parametrizable control module comprising first and second loadable counter, an electronic circuit	19981027	708/273
US 5828579 A	Scan segment processing within hierarchical scan architecture for design for test applications	19981027	716/2
US 5812417 A	Method and apparatus utilizing datapath line minimization to generate datapath floor plan for integi	19980922	716/9
US 5812414 A	Method for performing simulation using a hardware logic emulation system	19980922	716/16
US 5805860 A	Methods, data structures and apparatus for traversing a hierarchical netlist	19980908	716/12
US 5805859 A	Digital simulator circuit modifier, network, and method	19980908	703/16

US 5796623 A	Apparatus and method for performing computations with electrically reconfigurable logic devices	19980818	703/23
US 5748875 A	Digital logic simulation/emulation system	19980505	714/29
US 5740071 A	Method and apparatus for selective shape adjustment of hierarchical designs	19980414	716/11
US 5734581 A	Method for implementing tri-state nets in a logic emulation system	19980331	703/15
US 5703789 A	Test ready compiler for design for test synthesis	19971230	716/4
US 5696771 A	Method and apparatus for performing partial unscan and near full scan within design for test appli	19971209	714/726
US 5692160 A	Temperature, process and voltage variant slew rate based power usage simulation and method	19971125	703/23
US 5691912 A	Method for entering state flow diagrams using schematic editor programs	19971125	716/11
US 5663900 A	Electronic simulation and emulation system	19970902	716/17
US 5661733 A	Automatic test insertion	19970826	714/726
US 5661662 A	Structures and methods for adding stimulus and response functions to a circuit design undergoin	19970826	716/16
US 5659716 A	Pipe-lined static router and scheduler for configurable logic system performing simultaneous com	19970819	703/23
US 5657241 A	Routing methods for use in a logic emulation system	19970812	716/16
US 5644498 A	Timing shell generation through netlist reduction	19970701	716/2
US 5633807 A	System and method for generating mask layouts	19970527	716/19
US 5625803 A	Slew rate based power usage simulation and method	19970429	703/14
US 5617327 A	Method for entering state flow diagrams using schematic editor programs	19970401	703/14
US 5612891 A	Hardware logic emulation system with memory capability	19970318	716/16
US 5603043 A	System for compiling algorithmic language source code for implementation in programmable hard	19970211	712/1
US 5586319 A	Netlist editor allowing for direct, interactive low-level editing of netlists	19961217	716/17
US 5550839 A	Mask-programmed integrated circuits having timing and logic compatibility to user-configured logi	19960827	714/724
US 5541850 A	Method and apparatus for forming an integrated circuit including a memory structure	19960730	716/18
US 5535342 A	Pld connector for module having configuration of either first PLD or second PLD and reconfigurat	19960709	710/315
US 5524244 A	System for dividing processing tasks into signal processor and decision-making microprocessor i	19960604	717/140
US 5499192 A	Method for generating logic modules from a high level block diagram	19960312	716/17
US 5497498 A	Video processing module using a second programmable logic device which reconfigures a first pr	19960305	710/104
US 5483461 A	Routing algorithm method for standard-cell and gate-array integrated circuit design	19960109	716/14
US 5471398 A	MTOL software tool for converting an RTL behavioral model into layout information comprising bo	19951128	716/21
US 5452239 A	Method of removing gated clocks from the clock nets of a netlist for timing sensitive implementatic	19950919	703/19
US 5452231 A	Hierarchically connected reconfigurable logic assembly	19950919	716/16
US 5448496 A	Partial crossbar interconnect architecture for reconfigurably connecting multiple reprogrammable	19950905	716/16
US 5422833 A	Method and system for propagating data type for circuit design from a high level block diagram	19950606	703/14
US 5402357 A	System and method for synthesizing logic circuits with timing constraints	19950328	716/12
US 5301318 A	Hierarchical netlist extraction tool	19940405	716/11
US 5287511 A	Architectures and methods for dividing processing tasks into tasks for a programmable real time s	19940215	717/106
US 5200580 A	Configurable multi-chip module interconnect	19930406	174/264
US 5197016 A	Integrated silicon-software compiler	19930323	716/8
US 5197015 A	System and method for setting capacitive constraints on synthesized logic circuits	19930323	716/12
US 5187784 A	Integrated circuit placement method using netlist and predetermined ordering constraints to produ	19930216	716/7
US 5185736 A	Synchronous optical transmission system	19930209	370/358
US 5155836 A	Block diagram system and method for controlling electronic instruments with simulated graphic di	19921013	703/23
US 5111413 A	Computer-aided engineering	19920505	703/14
US 5036473 A	Method of using electronically reconfigurable logic circuits	19910730	703/23
US 4922432 A	Knowledge based method and apparatus for designing integrated circuits using functional specifi	19900501	716/17
US 4868785 A	Block diagram editor system and method for controlling electronic instruments	19890919	345/440
US 6353915 B	Interconnected electronic components system evaluating method e.g. for circuit board assemblies	20020305	

US 5586319 A	Method of interactively editing netlist on computer - involves defining user commands, prompting u	19961217